MAT-6660US2 PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant:	M. Hayama et al.	: Art Unit:
Serial No.:	To Be Assigned	: Examiner:
Filed:	Herewith	:
For:	METHOD FOR FABRICATING A MULTILAYER CERAMIC SUBSTRATE (AS AMENDED)	:

DIVISIONAL OF:

Applicant:	M. Hayama et al.	: Art Unit: 2814
Serial No.:	09/173,288	: Examiner: A. Chambliss
Filed:	October 14, 1998	: Attn: Issue Branch
For:	METHOD FOR FABRICATING A MULTILAYER CERAMIC SUBSTRATE (AS AMENDED)	: Confirmation No.: 1587 : :

PRELIMINARY AMENDMENT

Assistant Commissioner for Patents
Washington, DC 20231

S I R :

Prior to examination, please amend the above-identified application as follows:

IN THE TITLE:

Please replace the Title beginning at page 1, line 1 of the Specification:

METHOD FOR FABRICATING A MULTILAYER CERAMIC SUBSTRATE

IN THE SPECIFICATION:

Please insert the following section at page 1, line 5 of the Specification:

CROSS-RELATED APPLICATIONS

This application is a Divisional application of U.S. Patent Application Serial No. 09/173,288, filed October 14, 1998.

IN THE DRAWINGS:

Please delete sheets "5/13", "6/13", and "7/13" and replace with the figures attached hereto.

IN THE CLAIMS:

Please cancel claims 1-12.

Please replace claims 15-21 with the following amended claims:

15. (As Amended) The multilayer ceramic substrate of claim 13, wherein a meshed pattern is provided in a part of said conductive pattern.

16. (As Amended) The multilayer ceramic substrate of claim 13, wherein a shield pattern is provided at an outer edge of said conductive pattern.

17. (As Amended) The multilayer ceramic substrate of claim 13, wherein said ceramic substrate is provided with a through hole filled with an electroconductive substance and burned, and said via is disposed on the through hole.

18. (As Amended) The multilayer ceramic substrate of claim 13, further comprising a dielectric layer formed on a part of said ceramic substrate.

19. (As Amended) The multilayer ceramic substrate of claim 13, further comprising an LSI chip mounted on a part of one of said first and second conductive patterns with the face down and electrically connected.

20. (As Amended) The multilayer ceramic substrate of claim 13, further comprising an LSI chip mounted on a part of one of said first and second conductive patterns with the face down and electrically connected through an electroconductive paste applied on the top of a fine bump provided on one of said first and second conductive patterns, said fine bump formed by using a second groove which is disposed on said intaglio at a place corresponding to a pad of said LSI chip

21. (As Amended) The multilayer ceramic substrate of claim 13, further comprising an LSI package mounted on a part of one of said first and second conductive patterns with the face down and electrically connected through a lattice of lands with a pitch of not larger than 0.8mm, said lattice provided on one of said first and second conductive patterns.

Please add the following new claims:

22. (Newly Added) The multilayer ceramic substrate of claim 14, wherein a meshed pattern is provided in a part of said conductive pattern.

23. (Newly Added) The multilayer ceramic substrate of claim 14, wherein a shield pattern is provided at an outer edge of said conductive pattern.

24. (Newly Added) The multilayer ceramic substrate of claim 14, wherein said ceramic substrate is provided with a through hole filled with an electroconductive substance and burned, and said via is disposed on the through hole.

25. (Newly Added) The multilayer ceramic substrate of claim 14, further comprising a dielectric layer formed on a part of said ceramic substrate.

26. (Newly Added) The multilayer ceramic substrate of claim 14, further comprising an LSI chip mounted on a part of one of said first and second conductive patterns with the face down and electrically connected.

27. (Newly Added) The multilayer ceramic substrate of claim 14, further comprising an LSI chip mounted on a part of one of said first and second conductive patterns with the face down and electrically connected through an electroconductive paste applied on the top of a fine bump provided on one of said

first and second conductive patterns, said fine bump formed by using a second groove which is disposed on said intaglio at a place corresponding to a pad of said LSI chip.

28. (Newly Added) The multilayer ceramic substrate of claim 14, further comprising an LSI package mounted on a part of one of said first and second conductive patterns with the face down and electrically connected through a lattice of lands with a pitch of not larger than 0.8mm, said lattice provided on one of said first and second conductive patterns.

Respectfully Submitted,

Lawrence E. Ashery, Reg. No. 34,515
Attorney for Applicants

LEA/lm
Enclosure: Version With Markings Showing Changes Made
Dated: February 12, 2002
P.O. Box 980
Valley Forge, PA 19482-0980
(610) 407-0700

The Assistant Commissioner for Patents is hereby authorized to charge payment to Deposit Account No. 18-0350 of any fees associated with this communication.

EXPRESS MAIL Mailing Label Number: EV050915633US
Date of Deposit: February 12, 2002

I hereby certify that this paper and fee are being deposited, under 37 C.F.R. § 1.10 and with sufficient postage, using the "Express Mail Post Office to Addressee" service of the United States Postal Service on the date indicated above and that the deposit is addressed to the Assistant Commissioner for Patents, Washington, D.C. 20231.

Kathleen Libby

VERSION WITH MARKINGS TO SHOW CHANGES MADE

TITLE:

Specification at page 1, line 1:

~~MULTILAYER CERAMIC SUBSTRATE AND METHOD FOR FABRICATING THE SAME~~METHOD FOR FABRICATING A MULTILAYER CERAMIC SUBSTRATE

SPECIFICATION:

Specification at page 1, line 5:

CROSS-RELATED APPLICATIONS

This application is a Divisional application of U.S. Patent Application Serial No. 09/173,288, filed October 14, 1998.

CLAIMS:

15. (As Amended) The multilayer ceramic substrate of [either] claim 13 [or claim 14], wherein a meshed pattern is provided in a part of said conductive pattern.

16. (As Amended) The multilayer ceramic substrate of [either] claim 13 [or claim 14], wherein a shield pattern is provided at an outer edge of said conductive pattern.

17. (As Amended) The multilayer ceramic substrate of [either] claim 13 [or claim 14], wherein said ceramic substrate is provided with a through hole filled with an electroconductive substance and burned, and said via is disposed on the through hole.

18. (As Amended) The multilayer ceramic substrate of [either] claim 13 [or claim 14], further comprising a dielectric layer formed on a part of said ceramic substrate.

19. (As Amended) The multilayer ceramic substrate of [either] claim 13 [or claim 14], further comprising an LSI chip mounted on a part of one of said first and second conductive patterns with the face down and electrically connected.

20. (As Amended) The multilayer ceramic substrate of [either] claim 13 [or claim 14], further comprising an LSI chip mounted on a part of one of said first and second conductive patterns with the face down and electrically connected through an electroconductive paste applied on the top of a fine bump provided on one of said first and second conductive patterns, said fine bump formed by using a second groove which is disposed on said intaglio at a place corresponding to a pad of said LSI chip

21. (As Amended) The multilayer ceramic substrate of [either] claim 13 [or claim 14], further comprising an LSI package mounted on a part of one of said first and second conductive patterns with the face down and electrically connected through a lattice of lands with a pitch of not larger than 0.8mm, said lattice provided on one of said first and second conductive patterns.

Claims 1-12 have been cancelled.

Claims 22-28 are newly added.

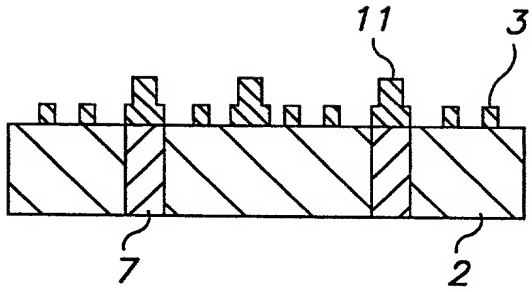

FIG. 10(a)

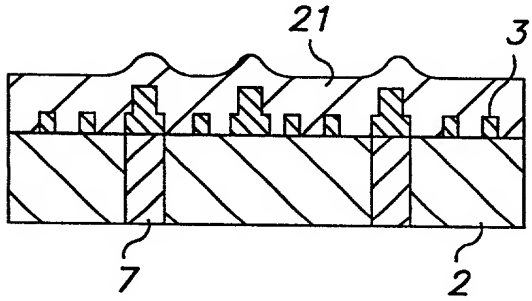

FIG. 10(b)

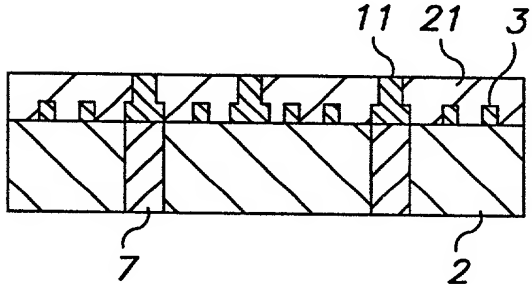

FIG. 10(c)

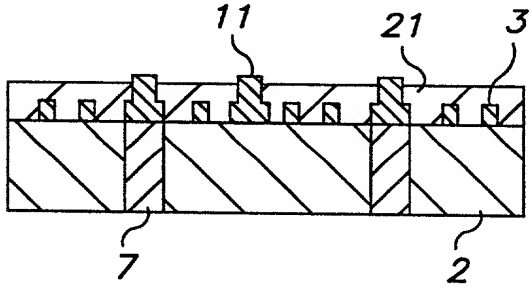

FIG. 10(d)

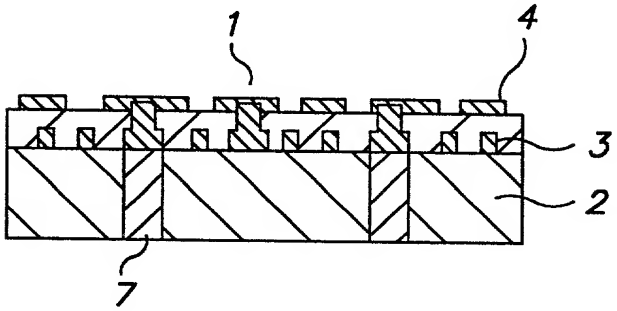

FIG. 10(e)

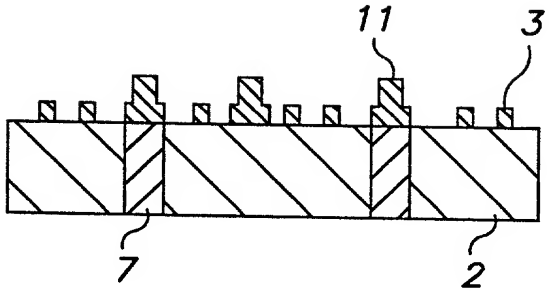

FIG. 11(a)

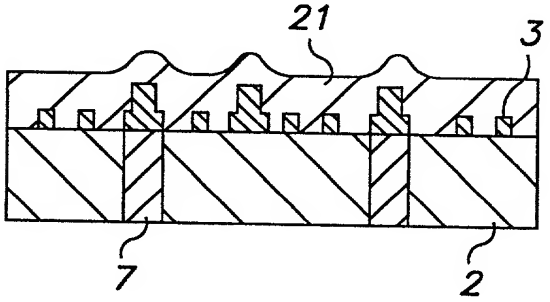

FIG. 11(b)

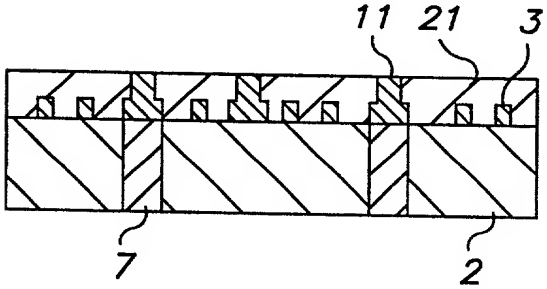

FIG. 11(c)

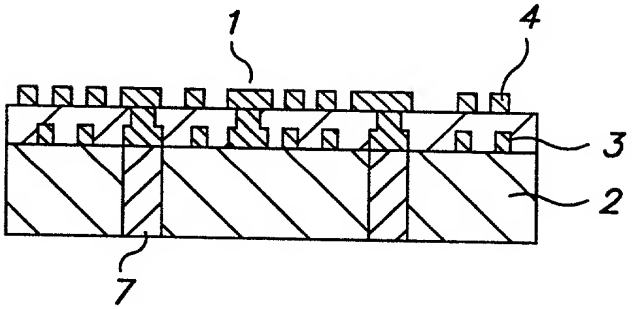

FIG. 11(d)

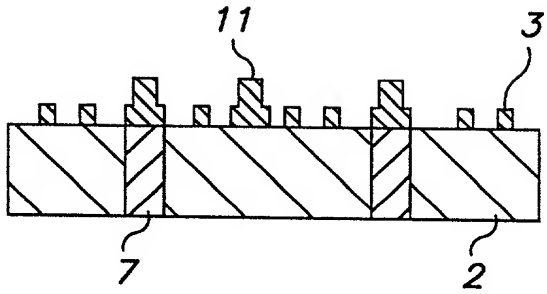

FIG. 12(a)

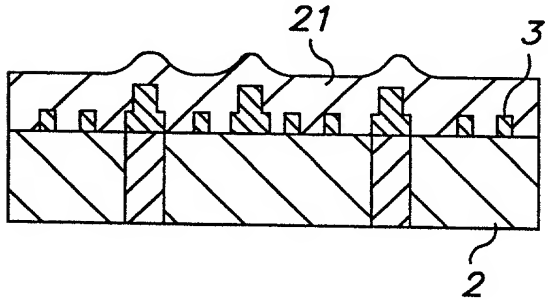

FIG. 12(b)

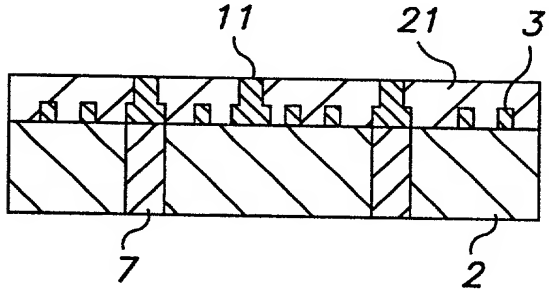

FIG. 12(c)

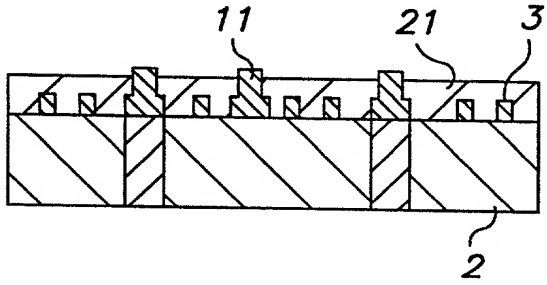

FIG. 12(d)

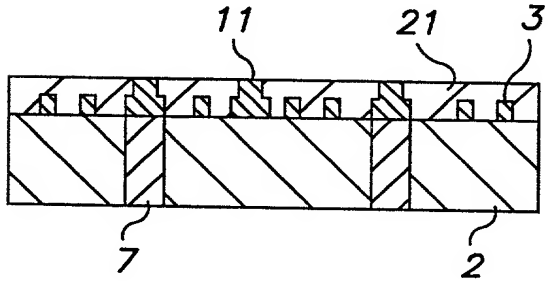

FIG. 12(e)

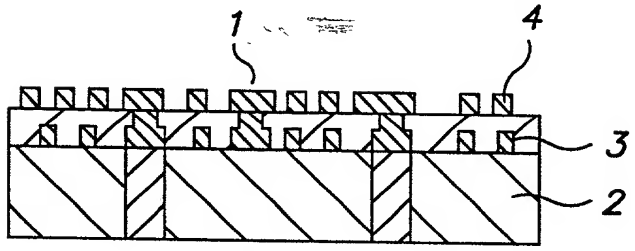

FIG. 12(f)